



RoHS

Implementation & Eco Design
Experience Sharing
CDIL

What is RoHS ?

Directive 2002/95/EC of the European parliament and of the council (27 January 2003)

Member States shall ensure that, from 1st July 2006, new electrical and electronic equipment put on the market does not contain

1. Lead,
2. Mercury,
3. Cadmium,
4. Hexavalent Chromium
5. Polybrominated biphenyls (PBB)
6. Polybrominated diphenyl ethers (PBDE).

Supply Chain Environment Management [Implications of EU's RoHS & WEEE Directives]

- # In 2001 CDIL carried out a joint study with ELCINA (Electronic Component Industries Association, India); NetPEM (Network for Preventive Environment Management) a Nagpur based NGO and IIIIEE (International Institute for Industrial Environmental Economics) Lund University, Lund, Sweden to understand the implications of European Union RoHS & WEEE Directives on Indian Electronic Components Manufacturers (with special reference to CDIL)
- # Prof. Lars Hansson & Prof. Thomas Lindqvist of Lund University Sweden visited CDIL to facilitate the understanding of the product oriented environment legislations in specific and the study as a whole
- # Prof. Hansjorg Griese of Fraunhofer Institute Berlin also visited CDIL and have facilitated in building understanding of GREEN ELECTRONICS
- # The outcome of this study and the understanding build up was disseminated in a seminar organized by ELCINA in 2002 among the member industries.

CDIL's RoHS Issues

Five Key Challenges of CDIL semiconductor devices with respect to RoHS compliance

- Elimination of RoHS material from process
- Development of alternative Material & Process particularly lead free process
- Forward & Backward Compatibility,
- Supply Chain Management,
- Cost of compliance,

Elimination of Chromium- The first step

Historically CDIL used Potassium Dichromate solution in HCl as pre cleaners in axial diodes prior to lead finish.

Action Taken : In Oct 2002 ,a non hazardous chemical MICROPREP 18 was tried and found as a substitute .

Result :

- Chrome eliminated from process.
- Customer demand was fulfilled.
- The Cost is reduced both Mfg. and Effluent Treatment Aprox. 1 lakh per year
- All the quality parameters are comparable.
- The solderability after dry aging and steam aging,
- Finish, Coverage , Solder thickness and Reliability results were found OK.

Cadmium in Ink- The Sony episode

In Jan 2003 Sony (India) awarded Green Partner status to CDIL.

In Oct 2002 CDIL found that the printing ink in the packaging of a consignment meant for Sony contained more than 9 ppm of Cadmium as per a test report from a Lab.

On probing it was found that the Lab was using BS EN 1122 : 2001 ["Plastics-Determination of cadmium - Wet decomposition method"]. This is done by Atomic Absorption Spectrometer (AAS)

On further investigation we found Inductively Coupled Plasma Atomic Emission Spectrometer [ICP-AES] is the more reliable instrument for such test. But this was available with Sony only. On contacting, Sony agreed to help us and It was found that there was error in the earlier report. Also the cadmium was found only in the refilled cartridge and not in the original cartridge.

Material & Process Development

CDIL has ADOPTED Lead free manufacturing
and all its devices have become lead free wef 1st July 2005.

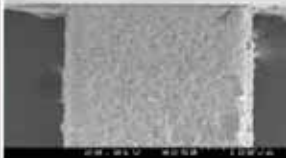
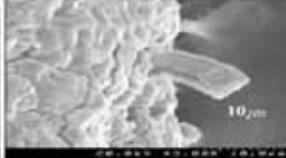
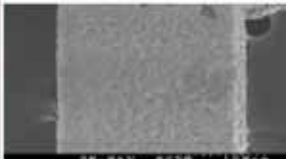
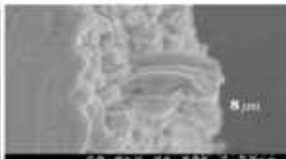
Earlier Terminal Finish : Sn/Pb--90/10

RoHS Compliant Lead free Terminal Finish : Matte Sn

Manufacturing issues to be addressed on an ongoing basis

- Growth of Tin whiskers
- Pb free solders typically have a higher melting point. The consequent **higher temperature processing** requires enhanced heat resistance in components and improvement/modification to PCB assembly equipment and materials.

Whisker Evaluation Test

Test Condition	Pure Tin Plating on Cu Lead Frame	
TCT (-55°C~+150°C)		
	1,000 cycle	
High Temperature High Humidity Storage (85°C/85%RH)		
	1,000 hr	

Phenomena of Whisker Growth

The ban on lead due to RoHS led to wide use of pure tin as an alternative to Tin Lead alloy that was earlier used as most popular solderable finish on semiconductor Terminations. But since 50's of the last century it was known that electroplated layers of tin and tin alloys show a certain propensity of uncontrolled growth of mono crystals of tin popularly known as **Tin whiskers**.

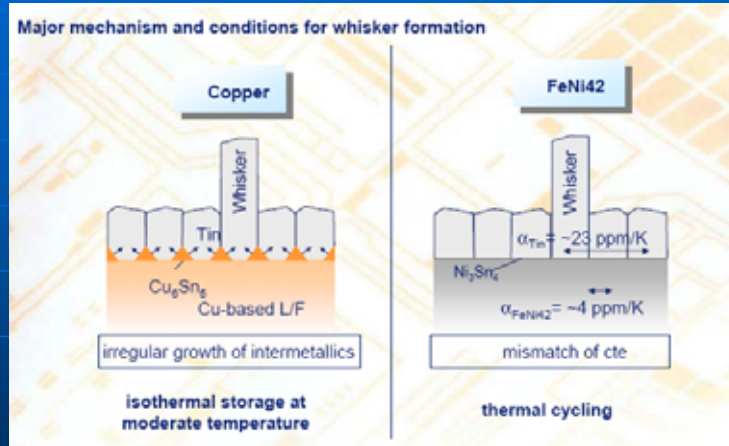


Phenomena of Whisker Growth

Years of research/investigations by various working groups lead to the following conclusion about the phenomenon:

- 1.The driving force of whisker formation is a compressive stress in the layer.
- 2.Whiskers grow from bottom.
- 3.Whiskers are mono crystals of Tin.
- 4.Whiskers can be straight, kinked, bended or of irregular shape.
- 5.Whisker propensity is influenced by alloying element in the tin alloy.
- 6.Whisker propensity is different for the various base materials on which the tin layer is deposited.

Phenomena of Whisker Growth



Whisker Mitigation

Matte Sn most preferred

Whisker mitigation -

Post plate (Matte Sn) bake – 150°C / 60 minutes
Developed and promoted by E4 – ST
Microelectronics, Philips Semiconductors, Infineon
Technologies, Freescale Semiconductors.

Applicable to Lead frames based on Cu and
Alloy 42 (FeNi42)

Mitigation of Whisker Growth

During the bake, the major effect is the artificial growth of the intermetallic double layer Cu_3Sn / Cu_6Sn_5 at the Cu – Sn interface.

This intermetallic grows uniformly at 150 deg C and forms a continuous layer, which acts as a diffusion barrier for further Cu – diffusion into Tin. This copper diffusion is associated with the intermetallic formation and happens only in the Tin grain boundaries at Room Temperature i.e. irregular growth of intermetallics.

At higher temperatures (150 C) there is a shift from grain boundary diffusion in favour of bulk diffusion resulting in a uniform layer. Since the intermetallic formation is associated with a volume increase, The irregularities induce stress and have to be avoided.

This can be achieved by introduction of barrier metals (Ni, Ag ...) or by the artificial growth of the inter metallic itself.

In addition, the phenomenon of recrystallization, dislocation slide and climb and recombination occur at 150 C resulting in a stress relieve.

Matte Tin has larger grains (> 1 micron) compared to Bright Tin (<0.5 micron). Smaller grains provide more grain boundaries leading to whiskering. Optimum grain size 2 – 5 micron. Also, carbon content should be <300 ppm.

In the FeNi42 Lead frame the whisker formation occurs during TMCL due to large CTE mismatch of FeNi42 and Sn.

SOLDER COMPATIBILITY

- **FORWARD COMPATIBILITY: COMPATIBILITY JUDGED WHEN COMPONENT FINISH IS NOT LEAD-FREE AND SOLDER USED IS LEAD-FREE**
- **BACKWARD COMPATIBILITY: COMPATIBILITY JUDGED WHEN COMPONENT FINISH IS LEAD FREE AND SOLDER USED IS NON LEADFREE**
- *All CDIL products, Pb-free & non Pb-free are Forward compatible and Backward compatible.*

“Green” Package

- A package is considered “Green” when four elements Pb, Br, Cl, Sb are not intentionally added during its manufacturing process. Although not specifically banned by legislation, Chlorine (Cl) is a halogen having the same toxicity as Br. Antimony in the form of Sb_2O_3 which is used as flame retardant on present day molding compounds is listed by the International Research of Cancer (IARC) as a carcinogen.
- Manufacturers consider the removal of the halogens (Cl + Br) and Sb necessary for making a package “Green”.
- The maximum level of the substances below for a “Green” package still has not been determined, however, industry consensus defines a “Green” Package to be :

“Green” Package

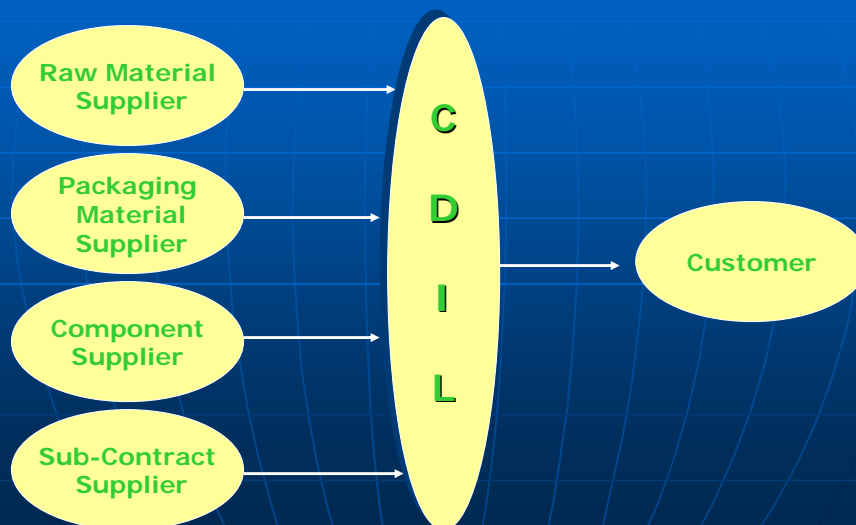
GREEN PACKAGE	SUBSTANCE	UPPER LIMIT	PACKAGE MATERIAL
Lead-Free	Pb	<1000ppm	Lead finish, Solder balls
Halogen-Free	Cl + Br	<900ppm	Mold Compound, Laminate, Solder resist
Antimony-Free	Sb_2O_3	<900ppm	Mold Compound, Laminate, Solder resist

Supply Chain Management

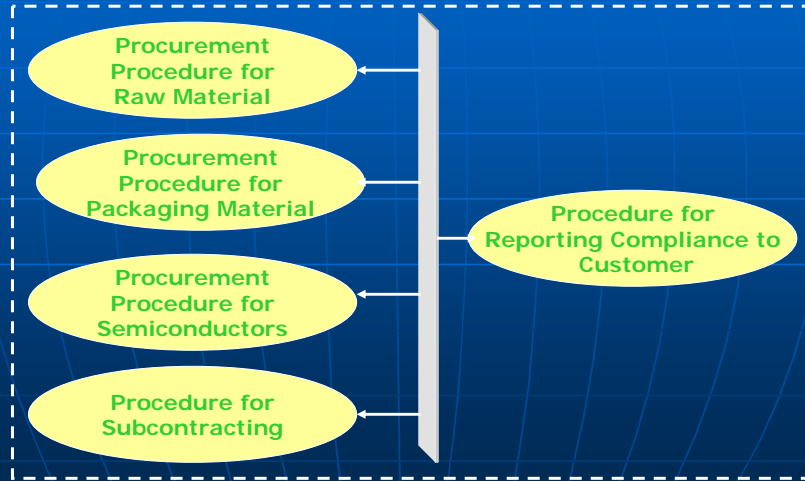
Supply Chain Environment

Management is the incorporation of environmental considerations into purchasing decisions and supplier management practices.

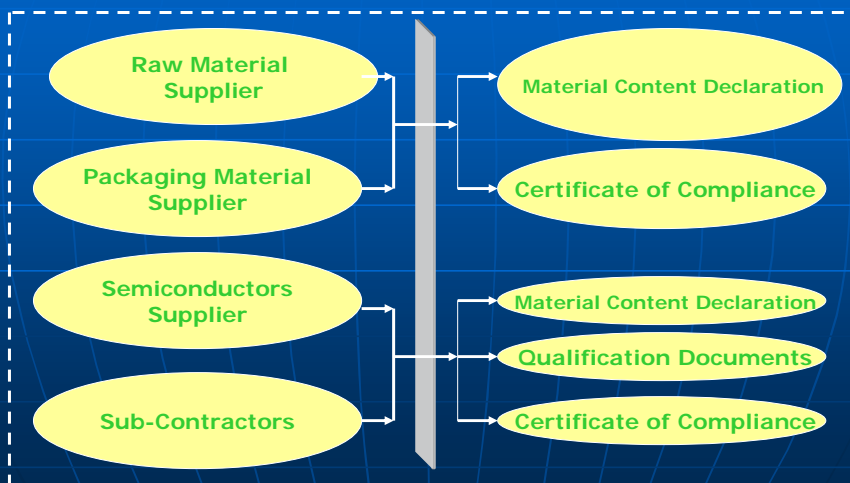
CDIL – Value Chain



System for Tracking & Reporting Compliance



System for Tracking & Reporting Compliance



Technical File



Format for Reporting Compliance to Customer

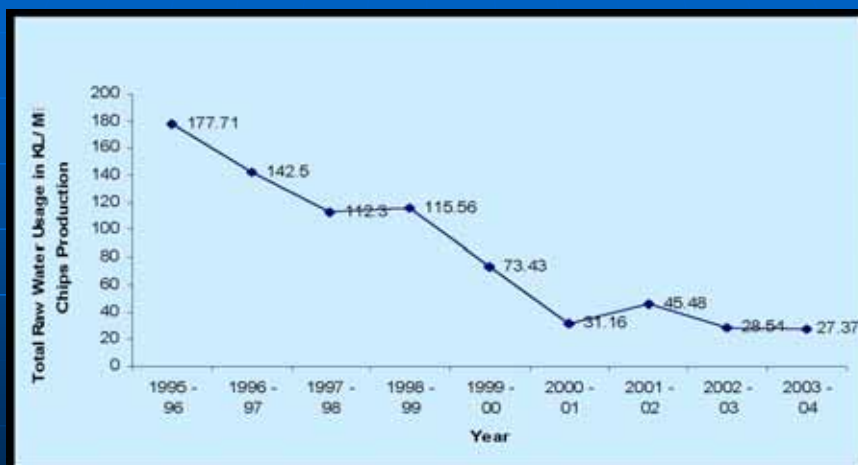
Package Name:

Package Weight:

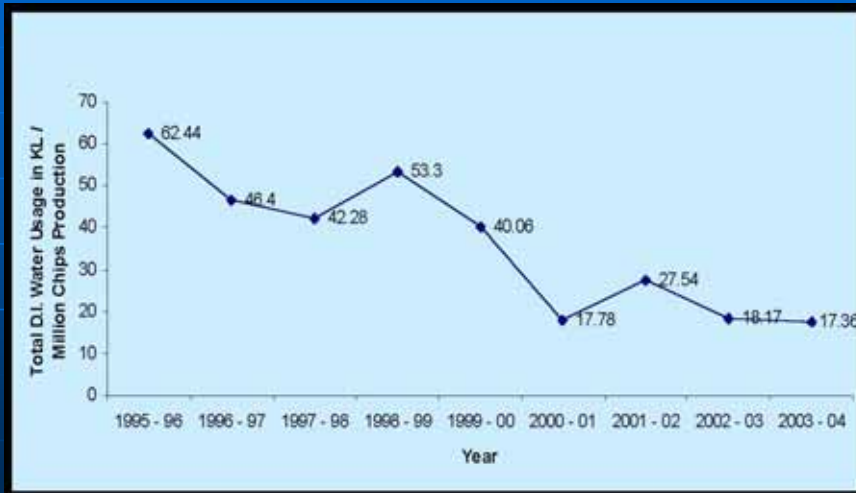
Material Content Declaration			RoHS / ELV Banned Substance Declaration (in mg/kg)						Remarks
Parts Name (Homogenous Material) & Weight (in mg)	Chemical Substance	Occurrence in %	Pb	Cd	Hg	Cr ⁶⁺	PBB	PBDE	

Initiative for Resource Conservation

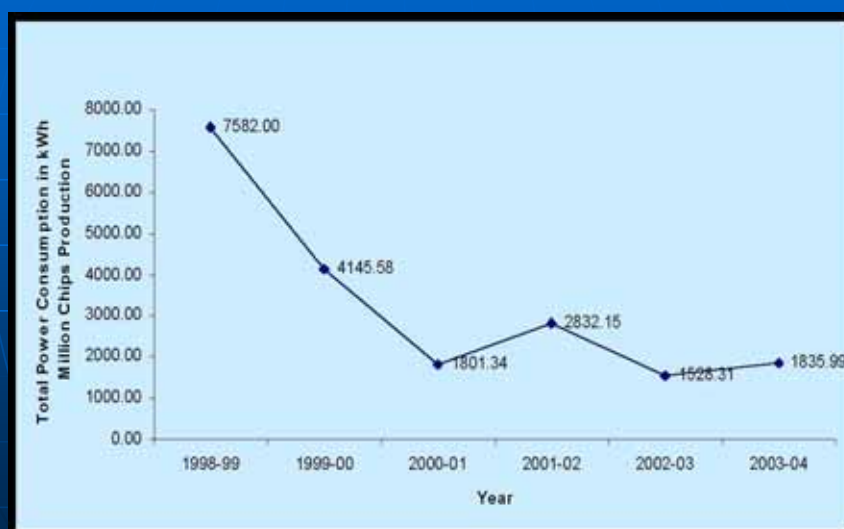
Total Raw water usage in KL / Million Chips Production



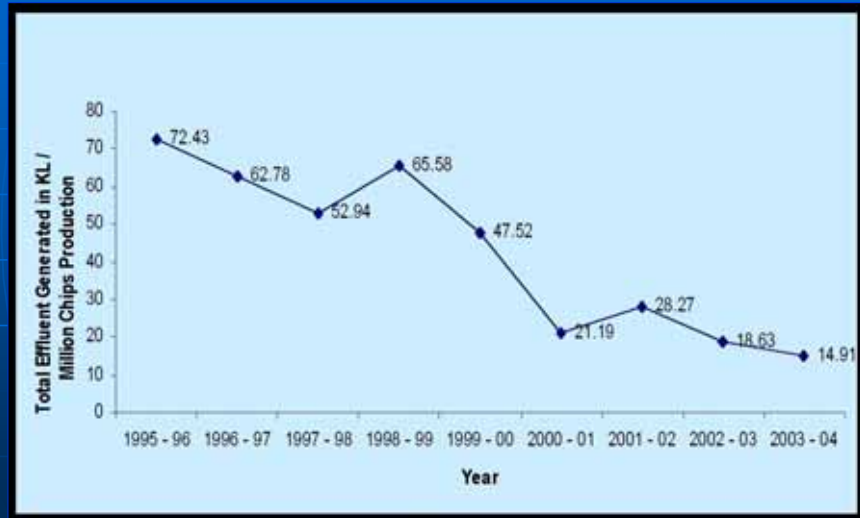
Total DI water usage in KL / Million Chips Production



Total Power Consumption in kwh / Millions Chips Production



Effluent Generated in KL/Million Chips Production



ENVIRONMENTAL
REPORTING

BACKGROUND

In view of heightened public and societal concern for environmental issues, the World Business Council for Sustainable Development (WBSCD) along with the Coalition for Environmentally Responsible Economics (CERES) has proposed the Global Reporting Initiative (GRI). The GRI was established in 1997 with a mission to elevate sustainability reporting to equivalency with financial reporting. In 2001, the Harvard Business School espoused the concept of the Triple Bottom Line (TBL) which comprises the three axes of People, Planet and Profits.

Several Indian companies have adopted TBL concepts in their Annual reports. The TBL is an adjunct to the earlier Balanced Score Card (BSC).

There are four constituents of Reporting :

- a) Quantitative burden
- b) Environmental accounting, including cost – benefit analysis (benefit includes Economic benefit and Environmental Impact Reduction).
- c) Qualitative listing of all initiatives in the area of Environment, Safety, Health and Social Contributions.
- d) Environment Cost analysis similar to Quality Cost

In due course the reporting of Quantitative Burden will become mandatory. The others are guidance for internal controls.

Understanding of Sustainability

Understanding of Sustainability



Ecological FootPrint Wafer Fabrication.

Environmental burden

The environmental burden method is used to estimate the potential environmental impact of emissions and wastes, rather than just stating quantities against local legislation limits.

This is an informative and scientifically sound way of quantifying the environmental performance of a company and can be used to set and monitor targets for improvement.

A total of 7 impact categories are used –Five dealing with emissions to air and two to water.

Environmental Burdens Wafer Fab (Comparison FY 04-05 and 05-06)

BURDEN	POTENTIAL EFFECTS	UNITS* (Per 1000 Wafer)	2004-05	2005-06
Global Warming	Climate change	Kg CO2 Eq	32972.0	27787.6
Ozone Depletion	Climate & health	Kg R-11 Eq	0.10	0.10
Total VOC emissions	Urban smog; health & safety	Kg VOC	94.3	92.2
Atmospheric acidification	Acid rain; health	Kg SO2 Eq	2.60	2.30
Photochemical Ozone Creation	Urban smog; health	Kg Ethylene Eq	1452.20	2086.30

Environmental Burdens Wafer Fab (Comparison 04-05 & 05-06)

BURDEN	POTENTIAL EFFECTS	UNITS* (Per 1000 Wafer)	2004-05	2005-06
Aquatic Oxygen Demand	Threat to fish and aquatic life	Kg BOD	15.70	15.10
Aquatic Eutrophication	Removes oxygen from water	Kg Phosphate Eq	7.40	7.10

* For meaningful control we need to monitor prorata e.g. MTCE/1000 wafers or MTCE / MReAV

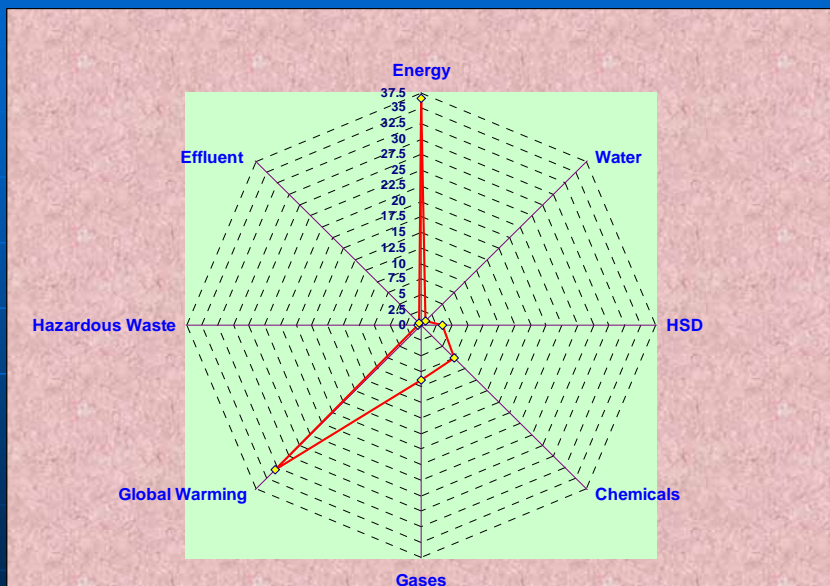
Wafer Fab. Environmental Impacts (Comparison FY 04-05 & FY 05-06)

Environmental Burden / Impacts	UNITS	Per wafer 2004-05	Per Wafer 2005-06
Global Warming	Kg CO2 Eq	32.972	27.788
Total VOC Emissions	Kg VOC	0.0943	0.0922
Ozone Depletion	Kg CFC-11 Eq	0.0001	0.0001
Atmospheric Acidification	Kg SO ₂ Eq	0.0026	0.0023
Photochemical Ozone Creation	Kg Ethylene Eq	1.452	2.0863
Aquatic Eutrophication	Kg Phosphate Eq	0.0074	0.0071
Aquatic Oxygen Depletion	Kg BOD	0.0157	0.0152

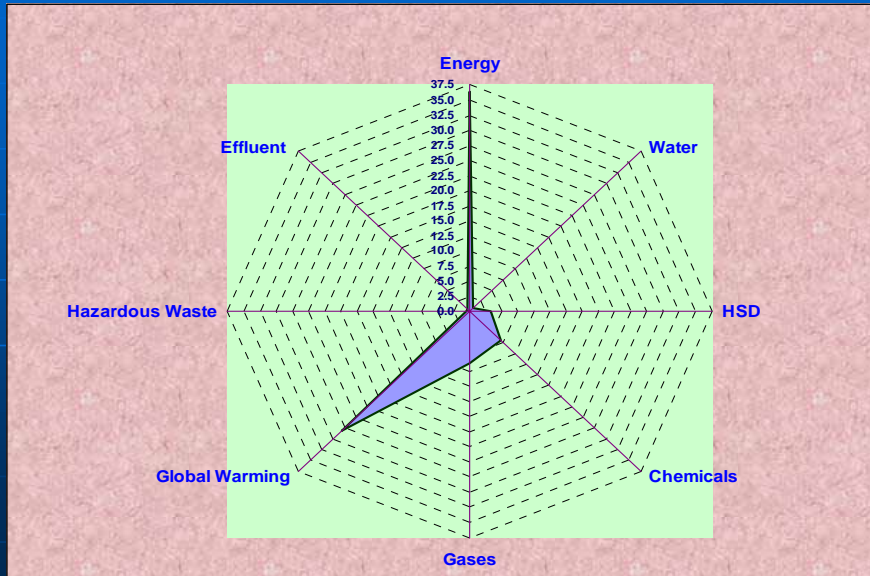
Wafer Fab. Resource Consumption (Comparison FY 04-05 & 05-06)

Resources Consumed	Units	Per Wafer (2004-05)	Per Wafer (2005-06)	%age Reduction
Energy	KWH	36.5	36.3	0.5%
HSD	Kg	3.4	3.2	5.9%
Water	KL	0.81	0.69	14.8%
Chemicals	Kg	7.505	6.63	11.7%
Gases	Kg	8.775	8.57	2.3%

ECO FOOT PRINT WAFER FAB (2004-05)



ECO FOOTPRINT WAFER FAB (2005-06)



Thank you